Claim 9 line 13 after "functions" insert --, wherein the connection layer implements input/output (I/O) circuits with different I/O functions by the sub-circuit cells in different positions--

Claim 13 line 1 after "claim" delete "~~8~~ 12" insert --9--

Claim 14 line 1 after "claim" delete "~~8~~ 12" insert --9--

Claim 15 line 1 after "claim" delete "~~8~~ 13" insert --9--

Lem 11/21/08

Allowable Subject Matter

7. Claims 1-3, 6-10, 13-15 are allowed.

8. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest forming a plurality of input/output sub-circuits cells with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas, wherein the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connections layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells among with all limitations of the claims 1 and 9.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."